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Effect of Additional Capacitor and Diode to A Single-Ended Primary Inductor Converter (SEPIC) Dc-Dc Converter For Offgrid System Based Photovoltaic (PV) Applications

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Abstract
For a stand-alone based photovoltaic (PV) applications, this article analyzes the implications of adding certain components to the single-ended primary inductor converter (SEPIC). A capacitor and a diode were added to the new topology's design. The added capacitor was used to boost and shaped the signal coming out from the power switch while the diode serves as a reverse back diode. The suggested topology showed that adding just two components to the standard SEPIC minimizes stress on the active components, particularly the power switch. Other advantages of the this methods are minimizing the value of duty cycle, extended voltage gain, less voltage stress over the power switch, a low density, and less cost. Following the realization of this new topology, a laboratory prototype was created to verify the viability of the new converter. A 125 V DC output was produced from a 12 V DC input using Matlab/Simulink.

Keywords: DC-DC SEPIC Converter, Voltage transfer ratio (voltage gain), Duty cycle, Voltage stress across the semiconductor components, and Photovoltaic (PV) panel

1.0 Introduction
Limiting the use of fossil fuels and maximizing the use of renewable energy resources as a source of electricity supply are necessary for a sustainable clean city. These plentiful resources hold great promise for the future because of their reversibility, simplicity of use, low maintenance requirements, and lack of environmental degradation. Solar energy is the most widely used renewable energy source in use today (Shaker and kraidi, 2019 ; Isah et al., 2019 ; Faraji et al., 2019; Isah et al., 2020).

Semiconductor materials used in photovoltaic (PV) panels absorb solar heat and transform it into electrical power (Asim et al., 2018 ; Oulad-abbou et al., 2019 ; Tewari and Ramesh-Babu, 2017). For optimal energy generation, the semiconductor cells on the panel are arranged in series or parallel (Saravani and Ramesh-Babu, 2017). Some of the major factors impacting their performance are tall buildings, little sunshine, trees casting shadows, and not having enough space for installation (Ahmad et al., 2019 ; Moral et al., 2019). Because PV generation typically produces low voltages, power converter technology is essential (Asim et al., 2018 ; Mitra and Rout, 2017 ; Krishna et al., 2017). The low DC voltage produced by the PV panel can be increased using this technology to reach the required output value (Gowtham et al., 2017; Mirzaei and Rezvanyvardom, 2017). Although there are many different kinds of power converters, a DC-DC type is needed at this point.

There are various types of DC-DC power converters, including transformerless and transformer-equipped models. Higher voltage gain can be obtained by adjusting the transformer's turn ratio and duty cycle, as both factors were judged to be too costly (Mirzaei and Rezvanyvardom, 2017). Some of the transformerless kinds' constructions have been well-utilized in the literature (Asim et al., 2018 ; Manuel et al., 2017 ; Revathi and Prabhakar, 2016 ; Dileep and Singh, 2017). The transformerless types just require a duty cycle to attain better voltage gains. The voltage gain of a traditional boost converter is consistently less than anticipated despite being transformerless and having a reasonable duty cycle.s

Only when a transformerless SEPIC is combined with a voltage doubler or another converter does it show promise (Saravanan and Ramesh-Babu, 2017; Sabzali et al., 2014). Buck-Boost behavior is shown by Zeta and Cuk converters, making them unsuitable for step-up applications (Bayat et al., 2019). The previously mentioned issues have prompted academics to look for other approaches.

Various transformerless DC-DC converter topologies have been extensively explored in the literature; however, some of these topologies have drawbacks, such as increased stress on the active components. Other topologies were constructed by combining two or three converters via cascade, inversion, or the addition of a voltage multiplier cell to attain increased voltage gain. Buck boost is a dependable duty-cycle method of increasing voltage gain (Krishna et al., 2017 ; Kaouane et al., 2016) however, the power switch's complexity is a little bit high. Double boost integrated with SEPIC is proposed in Kanimozhi et al., 2017 ; Kumar et al., 2017 but the large number of components has caused complications within the power switch. Cuk and boost converters were integrated in Kumar et al., 2017 ; Pires et al., 2017 ; Fernao et al., 2017 to solve similar problems but still, the inversion phenomena of the cuk converter caused some complications in the power switch. Additionally, a voltage multiplier cell boost was suggested in Saravanan and Ramesh-Babu, 2017 ; Mitra and Rout, 2017 ; Agrawal et al., 2017 ; Navamani et al., 2016; Napkin and Khawn-on, 2016 to optimize the system but the duty-cycle observed there is high enough to cause problem to the power switch.

This study presented a SEPIC with two additional components for PV panels along with other applications requiring a step-up conversion gain to supplement the current solutions. The advantages of the this methods are minimizing the value of duty cycle, extended voltage gain, less voltage stress over the power switch, a low density, and less cost. Following the realization of this new topology, a laboratory prototype was created to verify the viability of the new converter. A 125 V DC output was produced from a 12 V DC input using Matlab/Simulink.

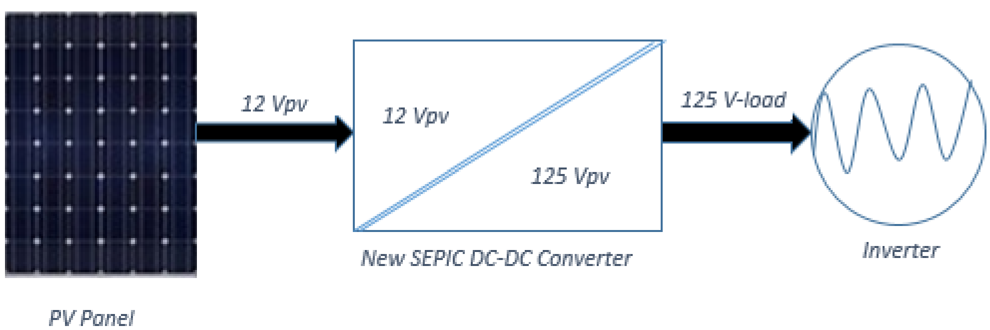

Figure 1: Architecture of the work showing the new SEPIC at the centre

2.0 Materials and Methods

Figure 2 shows the new architecture, which is made up of one adjustable power switch, three diodes D_1, D_2, & D_O, two inductances L_1 & L_2, and three capacitors C_1, C_2, & C_O. As can be observed, in comparison to the traditional SEPIC topology, the new converter has an extra diode and capacitor (D_1 & C_2). Because D_2 acts as a reverse recovery diode for the energy lost in Q, capacitor C_2 is positioned between the two diodes so that D_1 will block any discharged energy from the capacitor. As a result, C_1 will receive the blocked signal from C_2 and add it with the signal its received from the power switch and dissipate it through inductor L_2. This strategy resembles, but modifies, the techniques used in the classical boost converter described in Mitra and Rout, 2017 and SEPIC incorporated with a voltage doubler in (Saravanan and Ramesh-Babu, 2017). The modification involves replacing the about five components with only two components herein. Compared to the approaches used in the literature, the procedures used in this study are less expensive and more straightforward. The simulation was performed using Matlab/Simulink following the implementation of the new converter, and the laboratory setup was made ready. When the DX9 USB socket was connected to Trainer version 3371, all of the signals, presented in this work, were generated.

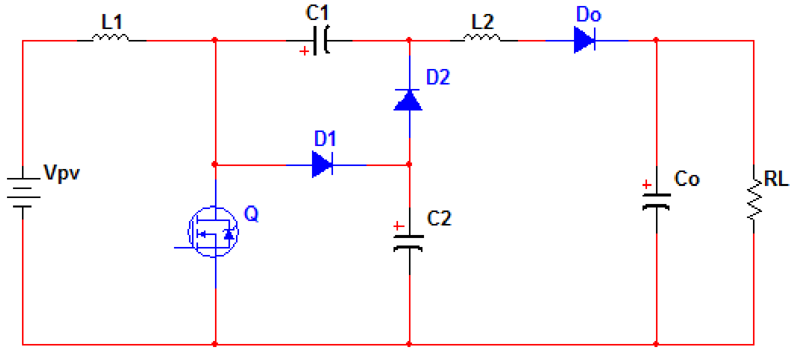

Figure 2: Proposed SEPIC Converter.

The new SEPIC converter's modes of operation are shown as follows:

Mode 1:
In the following, our power switch, represented by letter Q, is in ON-state. Therefore, the signal coming through inductor L_1 will deliver to diode $D_1$and then to the C_2. The signal in C_2 will be delivered to $C_1$and then to the output.

Mode 2:
In this mode, our power switch is in off-state, as such, the signal leak passes through inductor L_2.

2.1 Mathematical Equations of The New Converter viz:

$$V_{L1} = V_{PV} = V_Q \quad (1)$$

Equation (1) indicates that source voltage is the same with voltage in the inductor 1 and input of the power switch.

When the switching signal is applied to the power switch (Q), equation (1) becomes;

$$V_Q = V_{C2} = V_{C1}/2 = V_{PV}/(1-\partial) \quad (2)$$

Equation (2) means that, V_{C2} is blocked by diode D_1 and as such, it cannot discharge it signal. Therefore, V_{C1} will combine its own signal and that of V_{C2} and deliver it to the inductorL_2. ∂ represents the duty cycle.

Equation(2) can be used to evaluate the signal of the power switch or capacitorC_2.

This is to say, $V_{C1} = V_Q + V_{C2}$ (3)

For the output side of the circuit,

$$V_{Load} = V_{L2} = V_{DO} = V_{CO} = V_{C1} \quad (4)$$

OR, $V_{output} = V_{C1}$ (5)

When the switching signal is effected to the circuit in Fig. 2, the general input/output relationship of the circuit will take the following equation;

$V_{PV}\partial T = \left(V_{output} - V_{PV} - V_{C2}\right)(1-\partial)sT$ (6)

Thus, $V_{PV}\partial = \left(V_{L1} - V_{output}\partial - V_{PV} - V_{C2}\right)(1-\partial)$ (7)

Simplifying our equation (7) yields:

$\left(V_{output}(1-\partial) - V_{PV}(1-\partial)\right) - V_{C2} = 0$ (8)

From equation (2), which can be written as $V_{C2} = V_{PV}/(1-\partial)$, equation (8) can be deduced to;

$V_{output} = 2V_{C2}$ (9)

OR, $V_{output} = V_{CO} = V_{DO} = V_{C1} = 2V_{C2}$ (10)

To find the equation for the duty-cycle of the circuit, equation (10) can be written with respect to equation (2):

That is, $\partial = (V_{output} - 2V_{PV})/V_{output}$ (11)

Then, equation for the voltage transfer ratio (voltage gain A_V), it can be deduced from equation (7)

That is, $A_V = V_{Load}/V_{PV} = 2/(1-\partial)$ (12)

For the voltage stress within the power switch, equation (2) can also be used:

$V_Q = V_{PV}/(1-\partial)$ (13)

3.0 Design Parameters for The Proposed Sepic Converter

3.1. For the Inductance L_1 and L_2:

For the current ripple ($that\ is\ I_{L1}\ and\ I_{L2}$), two values were selected during the laboratory setup to design the inductanceL_1 & L_2. 4A and 6A were are the measured values. These values can be evaluated using equations(14) & (15).

$L_1 = (V_{PV}\ x\ \partial)/(f_s x I_{L1}) = 12$ mH (14)

$L_2 = (V_{c1}\ x\ \partial)/(f_s x I_{L2}) = 10$ mH (15)

3.2. Capacitors C_1 and C_O:

For input capacitor C1, input ripple voltage ΔV_{in} in equation(16) is adopted. But for capacitorsC_2& C_o, output ripple voltage ΔV_{Output}in equation (18) is adopted.

$\Delta V_{in} = (V_{PV})/(1-\partial)\,x10\% = 6\,V$ (16)

$\Delta V_{output} = (V_{PV})/(1-\partial) \quad = 62.5\,V$

As such, $C_1 = (I_O)/(f_s\ x\ \Delta V_{in}) = 2\ \mu$F (17)

For output capacitor Co,

$C_{output} = C_1 = (I_O)/(4\pi f_{grid} V_{LOAD} \Delta V_{LOAD}) = 16\ \mu$F (18)

Equation (18) can be used to calculate the output current (I_O).

That is; $I_O = C_1 x\ f_s\ x\ \Delta V_{in}$ (19)

Switching frequency of the new converter can be calculated with the following equation;

$f = 1/period = 20{,}000\ H_Z$ (20)

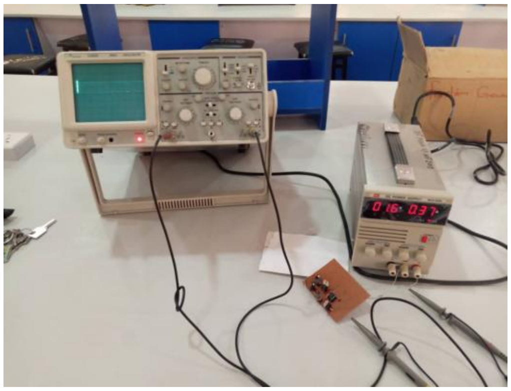

Figure. 3: Laboratory setup of the new converter.

4.0 Result and Discussions
4.1 Result

The calculated values of the components presented below were used in designing the proposed converter.

DC Output voltage, $V_{output} = 125\ V$
DC voltage source $V_{PV} = 12\ V$
Switching frequency, $f = 20{,}000\ Hz$
Duty cycle, $\partial = 0.8$
Power at the output $P_O = 100$ W
MOSFET (power switch) = IRFZ 44 N
Diodes models = $D_1 = D_2 = D_o$ = MUR 110

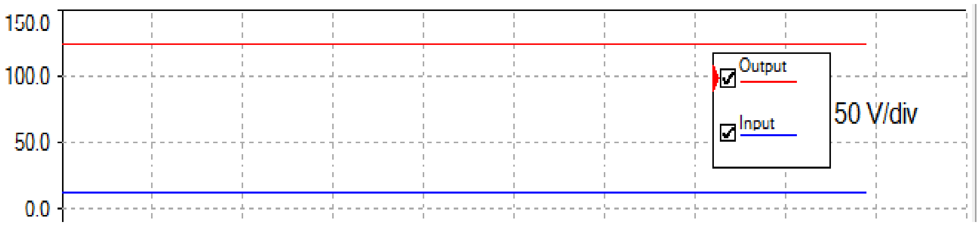

Figure 4: Output/Input signals of the proposed converter.

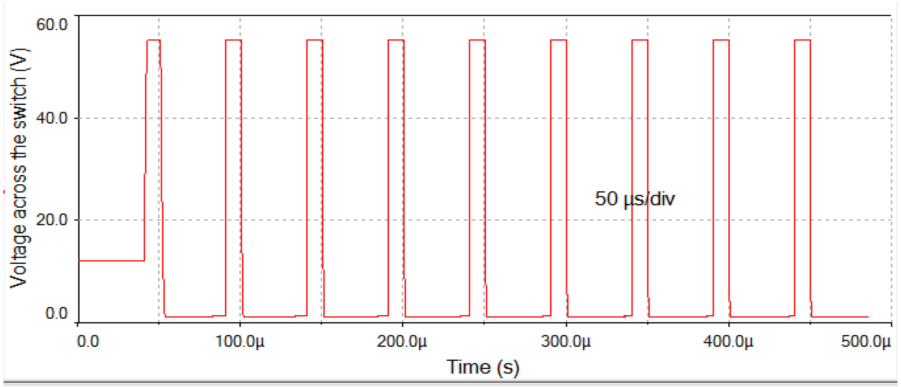

Figure 5: Voltage signal across the power switch (V_Q).

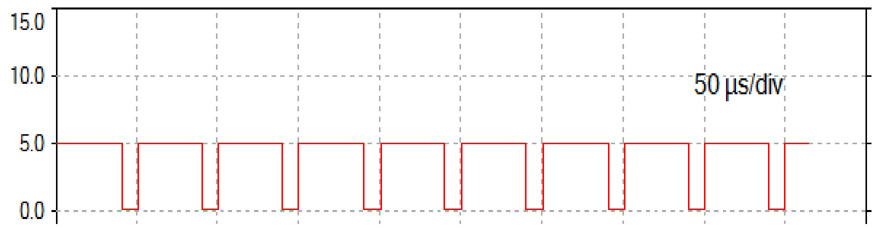

Figure 6: Voltage switching signal (V_{GS}).

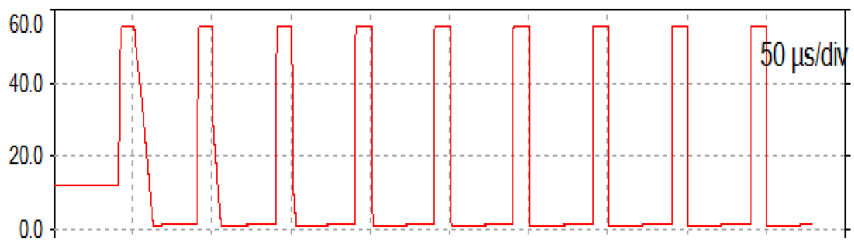

Figure 7: Voltage signal across diode (V_{D1}).

4.2 Discussions

Simulations:
The simulation was performed using Matlab/Simulink. With input and duty-cycle values of 12 V DC and 0.8, respectively, an output voltage of 125. 232 V DC was achieved. This indicates that a verified voltage gain value of 10.45 was obtained, following equation (12). About 50% of the voltage at the output should go through the power switch for a stress-free converter. A voltage along the active power switch of approximately 62.5 V, which can also be calculated using equation (13)

Experiment:
As seen in Fig. 3, the circuit prototype was constructed and tested in a lab. The signals displayed in Figures 4 and 5 were produced by a trainer (version 3371) linked via USB Dx9. In Figure 4, input/output signals are shown. It is evident that 125 V DC was generated from a 12 V DC input, resulting in a voltage gain of 10.42 with a duty-cycle value of 0.8. Equation (20) was utilized to determine the switching frequency by calculating the period of each oscillation, which is represented as 50 µs per division (or 100 µs per two divisions) in Figure 5. Illustration 6 shows the switching signal and Fig. 7 represents the signal of the diodeD_1. As seen in Fig. 8, the values acquired from the recently introduced SEPIC were contrasted with those from the conventional SEPIC.

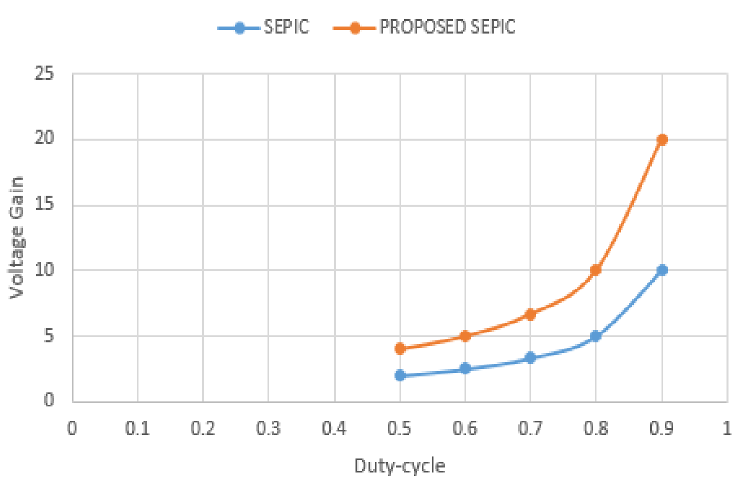

Figure 8: Comparison between voltage gain and duty-cycle of proposed SEPIC Converter.

5.0 Conclusion

This paper has presented the effects of adding capacitor and diode a SEPIC DC-DC converter for off-grid system-based PV panel applications. The novel structure has shown that the added components have eased the complications in the active components, especially the power switch way better than the integration methods and/or methods of incorporation with voltage multiplier. The voltage gain has also been extended widely at the expense of low-duty cycles.

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References

Agrawal, N., Gajpal, T., and Diwan, R., 2017. "High Gain DC-DC Converter with Voltage Multiplier using Pulse Generation," Int. J. Sci. Eng. Technol. Res., 6(4): 577–581.

Ahmad, R., Murtaza, A.R., and Ahmed, H., 2019. "Power tracking techniques for efficient operation of photovoltaic array in solar applications – A review," Renew. Sustain. Energy Rev., 101(2): 82–102. https://doi.org/10.1016/j.rser

Asim, A., Amir, A., Seng, H., El, A., and Abd, A., 2018. Comparative Analysis of High Voltage Gain DC-DC Converter Topologies for Photovoltaic Systems. Renew. Energy 18(2):163-167, https://doi.org/10.1016/j.renene.

Bayat, F., Karimi, M., and Taheri, A., 2019. "Robust output regulation of Zeta converter with load / input variations : LMI approach," Control Eng. Pract., 84(1):102–111. https://doi.org/10.1016/j.conengprac.

Dileep, G., and Singh, S.N., 2017. "Selection of non-isolated DC-DC converters for solar photovoltaic system," Renew. Sustain. Energy Rev., 76(1):1230–1247. http://dx.doi.org/10.1016/j.rser.

Faraji, R., Adib, E., and Farzanehfard, H., 2019. "Soft-switched non-isolated high step-up multi-port DC-DC converter for a hybrid energy system with minimum number of switches," Electr. Power Energy Syst., 106(2):511–519. https://doi.org/10.1016/j.ijepes.

Fernão, V., Foito, D., and Fernando, J., 2017. "A single switch hybrid DC / DC converter with extended static gain for photovoltaic applications," Electr. Power Syst. Res., 146: 228–235. http://dx.doi.org/10.1016/j.epsr.

Gowtham, S., Balaji, M., Harish, S., Pinto, M.S.A., and Jagadeesh, G., 2017. "Fault Tolerant Single Switch PWM DC-DC Converters for the Battery charging Appkications," in Energy Procedia, 117:753–760. http://dx.doi.org/10.1016/j.egypro.

Isah, H., Sagagi, Y.M., and Bako, A., 2019. "A Modified Boost-Boost High Gain DC-DC Converter for Photovoltaic (PV) Based Off- Grid Applications, "Nigerian Journal of Basic and Applied Sciences, 27(2):70–75, DOI://dx.doi.org/10.4314/njbas.v27i2.10

Isah, H., Sagagi, Y.M., and Tampul, H.M., 2020. "A Conventional Double Boost Converter with Voltage Multiplier Cell for Photovoltaic (PV) Applications," Savanna J. Basic Appl. Sci., 2(1):03–108.

Kanimozhi, G. et al., 2017. "Small Signal Modeling of a DC-DC Type Double Boost Converter Integrated With SEPIC Converter Using State Space Averaging Approach," in Energy Procedia, 117:835–846. http://dx.doi.org/10.1016/j.egypro.

Kaouane, M., Boukhelifa, A., and Cheriti, A., 2016. "Regulated output voltage double switch Buck-Boost converter for photovoltaic energy application," Int. J. Hydrogen Energy, 1–11, 2016. http://dx.doi.org/10.1016/j.ijhydene.

Krishna, N., Prashanth, M., Kumari, N.K., Krishna, D.S.G and Kumar, M.P., 2017. "Transformer Less High Voltage Gain Step-Up DC-DC Converter Using Cascode Technique," in Energy Procedia, 117:45–53. http://dx.doi.org/10.1016/j.egypro.

Kumar, M., Ashirvad, M., and Babu, Y.N., 2017. "An integrated Boost-Sepic- Ćuk DC-DC converter with high voltage The Boost-Sepic- Ćuk An integrated converter with high voltage ratio and reduced input current ripple." in Energy Procedia, 117:984–990. http://dx.doi.org/10.1016/j.egypro.

Manuel, J., Enrique, G., and Javier, A., 2018. "Theoretical Assessment of DC / DC Power Converters ' Basic Topologies . A Common Static Model," Appl. Sci., doi.org/10.3390/app8010019

Mirzaei, A., and Rezvanyvardom, M., 2017. "High voltage gain soft switching full bridge interleaved Flyback DC-DC converter for PV applications," Sol. Energy, 196(2): 217–227. https://doi.org/10.1016/j.solener.

Mitra, L., and Rout, U.K., 2017. "Performance analysis of a new high gain dc – dc converter interfaced with solar photovoltaic module," Reinf. Plast., 19(1): 63–74. http://dx.doi.org/10.1016/j.ref.2017.05.001.

Moral, D.L., Barrado, A., Sanz, M., Lázaro, A., Fernández, C., and Zumel, P., 2019. "Analysis and implementation of the Autotransformer Forward-Flyback converter applied to photovoltaic systems," Sol. Energy, 194(2): 995–1012. https://doi.org/10.1016/j.solener.

Nakpin A. and Khwan-On, S (n.d.) "A Novel High Step-up DC-DC Converter for Photovoltaic Applications," Procedia Comput. Sci., 86(1):409–412. http://dx.doi.org/10.1016/j.procs.

Navamani, J.D., Vijayakumar, K., and Jegatheesan, R., 2016. "Non-isolated high gain DC-DC converter by quadratic boost converter and voltage multiplier cell," Ain Shams Eng. J., http://dx.doi.org/10.1016/j.asej.

Oulad-abbou, D., Doubabi, S., and Rachid, A., 2019. "Power switch failures tolerance of a photovoltaic fed three-level boost DC- DC converter," Microelectron. Reliab., 92(2): 87–95, https:/doi.org/10.1016/j.microrel.

Pires, V.F., Foito, D., Baptista, F.R.B., and J. F. Silva, 2016. "A photovoltaic generator system with a DC / DC converter based Cuk topology on an integrated Boost-Cuk converter," Sol. Energy, 136(2): 1–9. doi.org/10.1016/j.solener.

Revathi, B.S., and Prabhakar, M., 2016. "Non isolated high gain DC-DC converter topologies for PV applications – A comprehensive review," Renew. Sustain. Energy Rev., 66:920–933, 2016. http://dx.doi.org/10.1016/j.rser.

Sabzali, A.J., Ismail, E.H., and Behbehani, H.M., 2014. "High voltage step-up integrated double Boost-Sepic DC-DC converter for fuel-cell and photovoltaic applications," Renew. Energy, pp. 1–10, 2014. http://dx.doi.org/10.1016/j.renene.

Saravanan, S., and Ramesh-Babu, N., 2017. "Analysis and implementation of high step-up DC-DC converter for PV based grid application," Appl. Energy, 190, 64–72. http://dx.doi.org/10.1016/j.apenergy.

Shaker, M. S. and Kraidi, A. A., 2019. "Robust observer-based DC-DC converter control," J. King Saud Univ. - Eng. Sci., 31(3): 238–244, 2019. https://doi.org/10.1016/j.jksues.

Tewari, N., and Sreedevi, V.T., 2018. A novel single switch dc-dc converter with high voltage gain capability for solar PV based power generation systems. Sol. Energy 171(1):466–477, https://doi.org/10.1016/j.solener.